AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph beginning on page 11, line 12, with the following rewritten paragraph:

--The data is streamed from the delay line 24 at the locations of the taps 26, 28, 30 through a bus 32 (e.g., PCI bus) to a plurality of processing blocks 34 located on the sound chip (Figs. 2 and 3). Each processing block [[34]] (54-58) receives data from a different tap point (26, 28, or 30) on the delay line 24. For example, processing block 54 receives data from tap point 26, processing block 56 receives data from tap point 28, and processing block 58 receives data from tap point 30. The processing block 34 includes a First-In/First-Out (FIFO) queue 36, a sample rate converter 38, and an audio processor 40 which modifies the signal to simulate effects such as attenuation, absorption, and environmental and positional effects. Gains are calculated in a geometry engine based on environment and position data and applied to the signal as it is passed through the audio processor 40. The sample rate converter 38 operates in conjunction with the delay line 24 as a time delay device which either increases or decreases the time delay of the output signals relative to the other signals output from the delay line 24, as further described below. The audio processor 40 and the sample rate converter 38 may be located together on a single chip, for example. The FIFO queue 36, sample rate converter 38, and audio processor 40 are preferably located on a single sound card which outputs a signal to a set of speakers or headphones.--

Please replace the paragraph beginning on page 17, line 9, with the following rewritten paragraph:

--In Fig. 4B, the delay between the direct path ~~signal~~ tap 50 and reflection ~~signal~~ tap 52 is reduced by 0.5 seconds. This is accomplished by increasing the step size of the reflection sample rate converter 56 from 0.5 to 0.75 to speed up the rate of consumption from 24 kHz to 36 kHz. The Base Step Size is still 0.5 for both taps. However, the ΔStep Size for the reflection ~~signal~~ tap 52 has been increased to 0.25. After one second has passed, the overall delay between output of the direct path ~~signal~~ tap 50 and the reflection ~~signal~~ tap 52 from the system will be 0.5 seconds.--

Please replace the paragraph beginning on page 18, line 3, with the following rewritten paragraph:

--During operation of the system, after the sound wave is started through the delay line 24, locations of the taps are compared to their desired location as determined by a desired delay. The desired delay is calculated in the host, based on information from the geometry engine, for example. If the delay provided by the [[tap]] delay line 24 is different than the desired delay, the step size of the sample rate converter 38 is adjusted to either increase or decrease the overall delay between the time the signal is input to the delay line buffer 24 and output from the processing block 34 (Fig. 3). The step size and rate of consumption are controlled by a feedback system which compares an actual delay of the signal by the system 20 to the desired delay. The step size is then adjusted within constraints on the allowable range of consumption rates to change the actual delay to the desired delay while limiting delay overshoot and oscillation, and preventing long term drift.--

Please replace the paragraph beginning on page 19, line 10, with the following rewritten paragraph:

--The following describes the control system shown in Fig. 5 with reference to the processing steps of the flowchart shown in Fig. 6. At each interrupt interval n, the host measures the actual delay for a particular tap by measuring the number of samples consumed by the sample rate converter 38, step 70 and the number of samples output by the sample rate converter, step 72. Actual delay is calculated from the measurements for number of samples output, output sample rate, number of samples consumed, and buffer sample rate, according to the above described equations. To reduce computational overhead, the number of samples output can be calculated less frequently, however, the estimation error will increase. The difference between the desired delay and the actual delay is the estimated delay error, step 74 (summation 62 of Fig. 5). The estimated delay error is used to calculate the step size, step 76 (block 64 of Fig. 5). The controller adjusts the consumption rate of the sample rate converter based on the new step size, step 78 (block 66 of Fig. 5). Audio processing continues with the new step size until it is reprogrammed at the next interrupt interval. The feedback control process is preferably

performed for each tap at each interrupt interval. While the number of samples consumed must be measured for each tap, the number of samples consumed need only be measured once per interrupt interval. To reduce the cost of feedback control computations, the interrupt interval may be reduced, however, the estimation error will increase.--